AMENDMENTS TO THE SPECIFICATION

Page 1:

In the title, please replace the original title with the following amended title:

MINIATURIZED VIRTUAL GROUNDING NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF

Page 21:

Please replace the paragraph beginning at line 23 with the following amended paragraph:

A method for manufacturing the memory cells will now be described with reference to Figs. 4 to 6 and Figs. 16 to 18.

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Please replace the paragraph beginning at line 20 with the following amended paragraph:

First of all, a shallow groove isolation region 102 for isolating the select transistor and peripheral circuit MOS transistor is formed on a p-type Si substrate 101 having a plane orientation (100). P well regions 104a, 104b, and 104c, N well regions 105a and 105b, and an isolation region 103 are formed by an ion implantation method (Fig. 4(a) and Fig. 16(a)). Next, channel ion implantation (not shown) is performed to adjust the threshold voltages for the memory cell, select transistor and peripheral circuit MOS

transistor. Then, ion implantation is conducted to form a diffusion layer (124 in Fig. 2 and Fig. 16(a-2)) under a third gate bind (125 in Fig. 2). Thanks to the above ion implantation, the memory cell diffusion layer wiring 113 and select transistor diffusion layer 120a can be electrically connected (Figs. 16 to 18). Next, an approximately 23 nm silicon oxide film 106, which serves as a high-voltage section gate dielectric film within the peripheral circuit region, is formed by thermal oxidation (Fig. 4(b) and Fig. 16(b)). Subsequently, a photoresist pattern is formed and then a wet etching method is applied to leave the silicon oxide film 106 in the high-voltage section of the peripheral circuit region (the silicon oxide film 106 is then designated by the reference numeral 106a) (Fig. 4(c) and Fig. 16(c)). Next, the photoresist pattern is removed, and then a 9 nm thermally oxidized film 108, which serves as a gate dielectric film for the select transistor and peripheral MOS transistor or a dielectric film for isolating the memory cell's third gate from the well, is formed by thermal oxidation in the low-voltage section of the peripheral circuit region and in the memory cell region. In this instance, the resulting thermally oxidized film thickness for the high-voltage section of the peripheral circuit region is 25 nm (the silicon oxide film 106a is then designated by the reference numeral 106b) (Fig. 4(d) and Fig. 16(d)). Subsequently, a polysilicon film 109 and a

silicon oxide film 110, which serve as the electrodes for the select transistor and peripheral MOS transistor or memory cell third gate, are sequentially deposited (Fig. 4(e) and Fig. 16(e)). A lithography and dry etching technology are then used to pattern silicon oxide films 110 and polysilicon films 109 (the silicon oxide films 110 and polysilicon films 109 are then designated by the reference numerals 110a, 110b and 109a, 109b, respectively). The employed pattern arrangement scheme is such that the silicon oxide films 110 and polysilicon films 109 in all non-memory-cell regions remain without being etched. Further, all the spaces formed by the patterning process are of the same dimensions to ensure that the word line polycide to be formed in a later process is uniformly embedded in the third gate space within the chip and in flat stepped form (Fig. 4(f) and Fig. 16(f)).

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Please replace the paragraph beginning at line 18 with the following amended paragraph:

Next, a silicon oxide film 111 is deposited d by low pressure CVD (Chemical Vapor Deposition) (Fig. 5(a) and Fig. 17(a)). This silicon oxide film 111 is then subjected to anisotropic etching so as to leave only the sidewall portion for the third gate pattern 109 (the silicon oxide film is

then designated by the reference numeral 111a) (Fig. 5(b) and Fig. 17(b)). The film provides protection to prevent the third gate oxide film from receding in a cleaning process before tunnel dielectric film formation, thereby letting the gate bird's beak grow to increase programming variations among cells and degrade the short channel characteristic of the third gate MOS. The thickness of the silicon oxide film 111 is set so that the film is completely removed in a cleaning process performed immediately before tunnel dielectric film formation but the amount of overetching is extremely small. Subsequently, arsenic tilt ion implantation and boron tilt ion implantation are performed in different directions to form a memory cell source/drain region 113 and punch-through stopper layer 112 (Fig. 5(c)). The diffusion layer 124 under the third gate is now connected to the memory cell source/drain region 113 (Fig. 17(c)). Next, the dielectric film 114 for isolating the floating gate from the well and the floating gate from the third gate is formed by thermal oxidation. The oxide film over the well is set to a thickness of 9 nm. In this instance, an approximately 20 nm oxide film 114a grows on the third gate sidewall (Fig. 5(d) and Fig. 17(d)). A polysilicon film 115, which serves as a floating gate, is then deposited d in such a manner as to incompletely fill the third gate space (Fig. 5(e) and Fig. 17(e)). A lithography and dry etching technology are then used to

pattern the deposited d film in a direction parallel to the third gate (the polysilicon 115 is then designated by the reference numeral 115a). The employed structure is such that an end of the floating gate pattern 115a is placed over the third gate 109a via the silicon oxide film 110a (Fig. 5(f) and Fig. 17(f)).

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Please replace the paragraph beginning at line 4 with the following amended paragraph:

Subsequently, a film stack of a silicon oxide film/silicon nitride film/silicon oxide film for isolating a floating gate from a word line, that is, an ONO film 116, a stack film of a polysilicon film and a tungsten silicide film serving as a word line, that is, a polycide 117, and a silicon oxide film 118 are sequentially deposited. In this instance, the thickness of the polysilicon film serving as a lower layer for the polycide 117 is adjusted so as to completely fill the memory cell space formed as indicated in Fig. 4(f) and make the surface of the polycide 117 nearly flat (Fig. 6(a) and Fig. 18(a)). Next, a publicly known lithography and dry etching technology are used to pattern the silicon oxide film 118 and polycide 117 to the minimum dimensions to accomplish word line formation (the silicon oxide film 118 and polycide 117 are then designated by the

reference numerals 118a and 117a, respectively). Further, the word line 117a is used as a mask to process the ONO film 116 and polysilicon film pattern 116a and finish the floating gate (the ONO film 116 and polysilicon film pattern 115a are then designated by the reference numerals 116a and 115b, respectively) (Fig. 6(b) and Fig. 18(b)). A lithography and drying etching technology are then used to pattern the silicon oxide film 110b and polysilicon film 109b in the peripheral circuit and form a gate electrode for the peripheral circuit MOS transistor (the silicon oxide film 110b and polysilicon film 109b are then designated by the reference numerals 110c and 109c, respectively) (Fig. 6(c)). The above process also forms a gate for the select transistor (127 in Fig. 2 and Fig. 18(c)). Further, at an end of the memory mat, the polysilicon film 109b and silicon oxide film 110b are patterned outside the word line 117a as shown in Fig. 2. Next, the low-concentration source/drain regions 119a, 119b, 120a, 120b are formed for the select transistor and peripheral circuit MOS transistor by an ion implantation method (Fig. 6(d) and Fig. 18(d)), a sidewall 121 for the silicon oxide film is formed, and then the high-concentration source/drain regions 122a, 122b, 123a, 123b are formed for the select transistor and peripheral circuit MOS transistor (Fig. 6(e) and Fig. 18(e)). This connects the diffusion layer 124 under the third gate, the source/drain region 113 for the memory cell, and the

diffusion layer ~~120b~~120a, 123a for the select transistor so that the memory cell source/drain is connected to the diffusion layer for the select transistor (Fig. 18~~(d)~~(e)). Subsequently, although not shown, an interlayer dielectric film is deposited and then contact hole (128 in Fig. 2) routed to a word line 117a, a gate electrode 127, 109c for the select transistor and peripheral MOS transistor, and the source/drain region 119a, 119b, 120a, 120b, 122a, 122b, 123a, 123b. A metal film is then deposited and processed to provide first layer metal wiring (129 in Fig. 2). Further, an interlayer dielectric film is formed and provided with a through-hole (130 in Fig. 2), and then second layer metal wiring (131 in Fig. 2) is formed to mainly provide a global bit line. In addition, an interlayer dielectric film is deposited and provided with a hole to form third layer metal wiring and then a passivation film to is formed to finish the nonvolatile semiconductor memory device.

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Please replace the paragraph beginning at line 23 with the following amended paragraph:

Further, the end of a memory cell array formed by the present invention has a significantly smaller number of word line open circuits/short circuits than the counterpart formed by the prior art. It means that the present

invention increases the yield. The reason is that the third gate, which provides a base for a word line, is subjected to line-and-space patterning in the memory cell array section only. As a result, the contact hole region for connecting the word line to the metal wiring is positioned over the polysilicon film 109b ~~the third gate 109a~~ and ~~the dielectric film 110a~~ the silicon oxide film 110b deposited on ~~the third gate 109a~~ the polysilicon film 109b so that the memory cell region is flush with the word line surface in the memory cell region. This increases the lithography focus margin for the word line to be patterned to the minimum dimensions, thereby enhancing the yield.